REMARKS

The Office Action dated April 24, 2007 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-17 are currently pending in the application, of which claims 1, 8-10, and 16-17 are independent claims. In view of the following Remarks, Applicant respectfully requests reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

The Office Action rejected claims 1-17 under 35 U.S.C. §102(e) as being allegedly anticipated by Herbst, *et. al.* (U.S. Patent No. 6,735,679). Applicant respectfully traverses this rejection for at least the following reasons.

Claim 1, upon which claims 2-7 are dependent, recites a method of receiving a packet, determining an address of a free entry in a queue, placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and placing packet data of the packet in a free entry of a first data structure. The method also includes one-to-one mapping between the queue and the first data structure.

Claim 8 recites a transmit queue system. The transmit queue system includes means for receiving a packet, means for determining an address of a free entry in a queue, means for placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and means for placing packet data of the packet in a free

entry of a first data structure. The transmit queue system also includes one-to-one mapping between the queue and the first data structure.

Claim 9 recites a transmit queue system. The transmit queue system includes a first data structure capable of holding a plurality of packet data, a queue capable of holding a linking list of addresses, a packet receiving engine capable of receiving a packet, a free entry engine coupled to the packet receiving engine and capable of determining an address of a free entry in the queue, a transmit queue engine, and a packet buffer engine. The addresses have a one-to-one mapping with addresses in the first data structure. The transmit queue engine is coupled to the queue, the packet receiving engine, and the free entry engine and is capable of placing the determined address in an entry of a prior-determined address in the queue to form a linking list. The packet buffer engine is coupled to the first data structure, the packet receiving engine, and the free entry engine and is capable of placing packet data of the packet in a free entry of the first data structure.

Claim 10, upon which claims 11-15 are dependent, recites a method of receiving an address in queue, reading packets from an entry from a first data structure with the same address as the received address, the queue, and the first data structure having one-to-one mapping, transmitting the packet data to a network node associated with the queue, reading a next address in the queue from the received address in the queue, and using the next address to repeat the reading packet data and the transmitting.

Claim 16 recites a transmit queue system. The transmit queue system includes means for receiving an address in a queue, means for reading packet data from an entry from a first data structure with the same address as the received address, means for transmitting the packet data to a network node associated with the queue, means for reading a next address in the queue from the received address in the queue, and means for using the next address to rerun the means for reading packet data and the means for transmitting. The queue and the first data structure have one-to-one mapping.

Claim 17 recites a transmit queue system. The transmit queue system includes a first data structure holding a plurality of packet data, a queue holding a linking list of addresses, and a packet transmit engine. The addresses have a one-to-one mapping with addresses in the first data structure. The packet transmit engine is coupled to the first data structure and the queue. The packet transmit engine is capable of receiving an address in the queue, reading packet data from an entry from the first data structure with the same address as the received address, transmitting the packet data to a network node associated with the queue, reading a next address in the queue from the received address in the queue, and using the next address to repeat the reading packet data and the transmitting.

As will be discussed below, Herbst fails to disclose or suggest every element of the claims, and therefore fails to provide the features discussed above.

Herbst discloses a method and apparatus for high performance switching in local area communications networks. In particular, Herbst relates to a new switching

architecture in an integrated, modular, single chip solution, which can be implemented on a semiconductor substrate such as a silicon chip (Abstract).

Applicant respectfully submits that Herbst fails to disclose or suggest every element recited in the pending claims. For example, Herbst fails to disclose or suggest "placing the determined address in an entry of a prior-determined address in the queue to form a linking list" and "one-to-one mapping between the queue and the first data structure" as recited in claim 1. Herbst also fails to disclose similar limitations recited in claims 8, 9, 10, 16, and 17.

Specifically, Herbst discloses switch-on-chip (SOC) 10 including a Common Buffer Memory Pool (CPB) 50, a Pipelined Memory Management Unit (PMMU) 70, and a Common Buffer Manager (CBM) 71 (See Figure 1; col. 5, lines 40-46). Packets, stored in the CBP 50, are typically stored as cells, rather than packets. PMMU 70 contains CBM 71 thereupon for which CBM 71 handles queue management and assigns cell pointers to incoming cells and common packet IDs (CPID) once the packet is fully written into CBP 50 (col. 7, lines 15-22).

Referring to Figure 8, Herbst discloses that when PMMU 70 determines that cell 112a is destined for an appropriate egress port on SOC 10, PMMU 70 controls the cell flow from Cell Protocol Sideband (CPS) Channel 80 to CBP 50. Once data packet 112 is received at PMMU 70 from CPS Channel 80, CBM 71 determines whether or not sufficient memory is available in CBP 50 for data packet 112. If sufficient memory is

available, CBM 71 places the data cell information into an assigned address in CPB 50, e.g. a free address within CPB 50 (col. 14, lines 29-45).

Herbst further discloses CBM 71 assigns cell pointers, which point first cell 112a to egress manager 76, which corresponds to the egress port to which data packet 112 will be sent after it is placed memory (*Id*). CBM 71 also assigns the CPID for data packet 112, which is used when data packet 112 is sent to destination egress port 24c (col. 14, lines 55-60). Herbst further discloses a linked list of memory pointers formed to define packet 112 when the packet is transmitted via appropriate egress port 24c (col. 14, lines 52-55).

But, Herbst fails to disclose or suggest at least "placing the determined address in an entry of a prior-determined address in the queue to form a linking list" and "one-to-one mapping between the queue and the first data structure" as recited in claim 1.

The Office Action alleges that Herbst discloses the aforementioned features. The Office Action states "the term cell pointers and Common Packet Identifier (CPID) corresponds to an address of a free entry in a queue." The Office Action further states "a linked list of memory pointers is formed which defines packet when the packet is transmitted via the appropriate egress port" corresponds to the formation of the linking list as recited in claim 1. The Office Action further states "cells of a particular packet are always handled together corresponds to one-to-one mapping between the queue and the first data structure." (See Office Action on pages 2-3).

Applicant respectfully disagrees with the Office Action's characterization of Herbst's teachings. Rather, as previously noted, Herbst discloses that when PMMU 70 determines that cell 112a is destined for an appropriate egress port on SOC 10, CBM 71 determines if sufficient memory is available in CPB 50 for data packet 112. If sufficient memory is available, CBM 71 places data cell information in a free assigned address in CPB 50 (col. 14, lines 29-45).

Cell pointers and CPID are not "addresses of a free entry in queue"; rather, they are identifiers used in managing or routing data cell 112 to the appropriate egress port via egress manager 76. Therefore, the Office Action's characterization of cell pointers and CPID as "addresses of a free entry in queue" is improper.

Further, Herbst discloses a linked list of *memory pointers*, or identifiers, formed to define packet 112 when packet 112 is transmitted via egress port 24c (col. 14, lines 52-55), but fails to disclose or suggest "placing the *determined address* in an entry of a *prior-determined address* in the queue to forming a linking list" as recited in claim 1. As previously noted, cell pointers, memory pointers, and CPID are not "an address of a free entry in a queue." Therefore, it would be improper to conclude that forming a linked list of *memory pointers* is "placing the determined address in an entry of a prior-determined address in the queue to form a linking list" as recited in claim 1.

Further, Herbst fails to disclose "one-to-one mapping between the queue and the first data structure." As previously noted, Herbst discloses a free address pool that provides storage and identification information for data packet 112 in CPB 50 (col. 14,

lines 34-36). Herbst also discloses that cells of a particular packet are always handled together to avoid corruption of packets (col. 12, lines 16-18), which merely denotes that cells associated with a particular data packet 112 are handled together when data packet 112 flows from CPS Channel 80 to CPB 50. Accordingly, Applicant respectfully submits that the Office Action's citation fails to demonstrate that Herbst discloses or suggests "one-to-one mapping between the queue and the first data structure" as recited in claim 1.

For similar reasons, Applicant respectfully submits that Herbst fails to disclose or suggest every element recited in claims 8, 9, 10, 16, and 17.

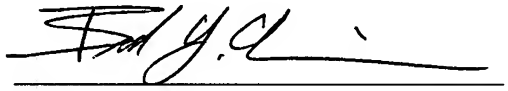
Accordingly, Herbst fails to disclose or suggest every element recited in claims 1, 8, 9, 10, 16, and 17. As such, Applicant respectfully requests that the rejections of claims 1, 8, 9, 10, 16, and 17 be withdrawn. Claims 2-7 and claims 11-15 are dependent upon claims 1 and 10, respectively. Accordingly, claims 2-7 and 11-15 should be should be allowed at least for their dependence upon claims 1 and 10, respectively, and for the specific limitations recited therein.

Accordingly, Applicant respectfully requests withdrawal of the 35 U.S.C. §102(e) rejection of claims 1-17. Applicant respectfully submits that claims 1-17 are allowable.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Brad Y. Chin
Registration No. 52,738

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

BYC:jf